REMARKS

Reconsideration of this application as amended is respectfully requested. No new matter has been added. Claims 1-36 remain pending.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 2, 5, 6, 18, 19, 21, 23, 24, 30, 31, 34 and 35 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 5,615,358 to Vogley et al. ("Vogley"). Applicant respectfully disagrees with the reasons for rejection.

Claim 1 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus.

Vogley discloses a data processing system including a time skewing circuit (26) for adjusting a delay of address and control signals "so that they *concur* in arrival time, at the synchronous memory devices 30 or at locations within the time skewing circuit 26, with arrival of data bits after transmission over leads of fixed but *different lengths*" (Vogley, col. 6 lines 46-51, col. 5 lines 51-65, emphasis added). Applicant submits that Vogely's different delay times, applied to the address and control signals correspond to the different *lengths* of the memory data bus (28) across which the data bits must propagate. However, nowhere does Vogely disclose or suggest a first data bus having "a first data bus *symbol time* that is *shorter* than a first address and control bus symbol time of the first address and control bus," as recited in claim 1. Applicant submits that merely delaying the times at which buffered address and control signals are *output* onto memory address and control buses (27 and 60, respectively) does not affect a characteristic "symbol time" of the respective bus (Vogley, col. 5 lines 51-65 and col. 8 lines 30-45).

Applicant further submits that Vogley does not disclose a first data bus that "uses *differential* signaling," as recited in claim 1. Thus, for at least the foregoing reasons, applicant submits that Vogley does not disclose one or more limitations of cliam 1, and

therefore does not anticipate claim 1, nor dependent claims 2 and 30.

Claim 5 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus has a first data bus symbol time that is shorter than a first address and control bus symbol time of the first address and control bus and wherein the first address and control bus symbol time is shorter than a first clock signal cycle time of the first clock signal.

Applicant submits that, for at least the reasons given above with respect to claim 1, Vogley does not disclose the above-recited limitation of claim 5. Therefore, Vogley does not anticipate claim 5, nor dependent claims 6 and 31.

Claim 18 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first data bus uses differential signaling and wherein the first memory component accesses a first word stored in the first memory component, the first word being wider than a first data bus width of the first data bus.

Applicant submits that Vogley does not disclose the above-recited limitation. Even assuming *arguendo* that the data bus (28), of Vogley, can send data of varying lengths and sizes, as suggested in the Office Action, Vogley still does not disclose *a first memory component* to access "a first word stored in the first memory component, the first word being *wider* than a first data bus width of the first data bus," as recited in claim 18. Therefore, applicant submits that Vogley does not anticipate claim 18, nor dependent claims 19 and 34.

Claim 21 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller includes a first receive circuit having a first read

> timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first data bus uses differential signaling.

Vogley discloses a write/read enable circuit (101) for generating read enable signals based on a read delay code, wherein "when the data processing system 15 of Fig. 1 is being setup, the appropriate read delay code is applied to each read enable delay register and selector... this read enable data *remains* stored therein as long as the data processing system 15 is energized" (Vogley, col. 7 lines 44-65). Applicant submits that once the data processing system 15 is setup, the amount of delay applied to the read enable signals does not change. Thus, nowhere does Vogley suggest or disclose "a first read timing adjustment subcircuit for *adjusting* a first adjustable read data sampling time point for first read data sampled from the first data bus," as recited in claim 21. Applicant therefore submits that Vogley does not anticipate claim 21, nor dependent claims 23, 24 and 35.

Claim Rejections - 35 U.S.C. § 103

Claims 9, 11, 13, 14, 16, 17, 25, 27, 28, 29, 32, 33 and 36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Vogley in view of U.S. Patent No. 5,530,523 to Sanwo et al. ("Sanwo"). Applicant respectfully disagrees with the reasons for rejection.

Claim 9 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus and wherein the first data bus has a first data bus symbol time that is shorter than a first address and control symbol time of the first address and control bus.

Applicant submits that, for at least the reasons given above with respect to claim 1, Vogley does not disclose the above-recited limitation of claim 9. Applicant further submits that Sanwo also does not disclose the above-recited limitation. Accordingly,

even if Vogley and Sanwo could be combined in the manner proposed in the Office Action, such combination would still lack at least the above-recited limitation, and therefore would not have rendered claim 9, nor dependent claims 11 and 13, obvious.

Claim 14 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory component includes a first termination structure connected to the first data bus, wherein the first data bus uses differential signaling, and wherein the first address and control bus does not use differential signaling.

Neither Vogley nor Sanwo discloses a memory system having a first data bus and a first address and control bus, "wherein the first data bus uses differential signaling, and wherein the first address and control bus does *not* use differential signaling," as recited in claim 14. Furthermore, although not explicitly stated in Vogley, it is understood by applicant that both the data bus and the address bus use the *same* (e.g., differential) method of signaling (Vogley, Fig. 12). Thus, even if Vogley and Sanwo could be combined in the manner proposed in the Office Action, such combination would still lack at least the above-recited limitation, and therefore would not have rendered claim 14, nor dependent claims 16, 17 and 33, obvious.

Claim 25 recites, in part:

> a first data bus connected to the first memory controller and to the first memory component, wherein the first memory controller component includes a first receive circuit having a first read timing adjustment subcircuit for adjusting a first adjustable read data sampling time point for first read data sampled from the first data bus and wherein the first memory component includes a first termination structure connected to the first data bus.

Applicant submits that, for at least the reasons given with respect to claim 21, Vogley does not disclose the above-recited limitation. Applicant further submits that

Sanwo also does not disclose the above-recited limitation. Accordingly, even if Vogley and Sanwo could be combined in the manner proposed in the Office Action, such combination would still lack at least the above-recited limitation, and therefore would not have rendered claim 25, nor dependent claims 27-29 and 36, obvious.

Allowable Subject Matter

Applicant acknowledges that claims 3, 4, 7, 8, 10, 12, 15, 20, 22 and 26 have been indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, but respectfully declines to amend such claims at this time in view of the foregoing remarks.

In Conclusion

Applicant respectfully submits that all pending claims are in condition for allowance. If a telephone interview would be helpful in any way, the examiner is invited to call the undersigned attorney.

Authorization is hereby given to charge deposit account 501914 for any fee deficiency associated with this Amendment.

Respectfully submitted,

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